Remarks

Office Action dated June 22, 2004, objects to FIGURES 1, 2, and 3 and rejects all claims as anticipated by the US Pat. No. 5,974,579 to Lepejian st al. (herein "the Lepejian patent"). In response, amendments are made to FIGURES 1, 2, and 3 in accordance with suggestions in the Office Action and claim 1 is amended.

Claim 1 is rejected as anticipated by the Lepejian patent. In response, claim 1 is amended to include the limitation that "the memory element [has] a plurality of impermissible operations". The Lepejian patent is directed to a self test for embedded parallel memories of different sizes. See col. 4, lines 5-8. The only impermissible operation disclosed is the memory address overflow operation where a value on memory address lines exceeds the available addressable memory space. See col. 5, lines 19-29 and col. 7, lines 3-21. The Lepejian patent teaches a single bit, ADDR HALT, which arrests the address lines at a permitted value until a new permitted value is presented. Claim 1, as amended, however, recites accommodation of more than one impermissible operation where the "decoder accepting the test code and generating at least two output lines" …that "reflect a value"…"that when combined with respective memory access lines disables said impermissible operations". Accordingly, it is believed that claim 1 is

patentably distinct from the cited references and allowance is solicited.

Claims 2-6 are also rejected as anticipated. Claims 2-6 remain unamended. Claims 2-6 depend from claim 1 and for at least the same reasons claim 1, as amended, is believed to be patentable, claims 2-6 are also believed to be patentable and allowance is solicited.

Claim 7 is rejected as anticipated by the Lepejian patent. In response claim 7 is amended to recite in the preamble that the memory element has "a plurality of impermissible operations". Claim 7 also recites the step of "mapping said test code to at least two output lines" and is amended to recite that "the step of mapping causes said output lines to reflect values"...that "disable the impermissible operations". The Lepejian patent generates a single signal to halt the address or not depending upon the size of the memory under test. See Figure 1 and col. 5, lines 19-42. Embodiments of the method claimed in claim 7, however, are able to accommodate more than one impermissible operation. Scaling of the teachings to accommodate more than one impermissible operation is not taught or suggested by the Lepejian patent. Accordingly, it is believed that the method of claim 7, as amended, is patentably distinct over the cited references and allowance is solicited.

Claims 8-12 are rejected as anticipated by the Lepejian reference. Claims 8-12 remain unamended. Claims 8-12 depend from claim 7, which, as amended,

is believed to be patentable. Accordingly, claims 8-12 are believed to be patentable for at least the same reasons claim 7 is believed to be patentable and allowance is solicited.

Claim 13 is rejected as anticipated by the Lepejian patent. Claim 13 is amended to recite that the memory element has "more than one impermissible operation". This is distinct from that disclosed in the Lepejian patent because the Lepejian patent disclosed a plurality of memories where because the memories are of different sizes, there is a possibility of a value on the address lines exceeding the available memory space. See col. 4, lines 4-15. Claim 13 also recites "each decoder accepting said test code and generating at least two output lines for each memory element"...that "reflect a value that" operates to "disable[s] said impermissible operations". By contrast, the Lepejian patent discloses a single signal to halt an address access or not. See FIGURE 1, ADDR HALT 52 signal from ADDR FILTER 50, and col. 5, lines 19-29. Accordingly, it is believed that claim 13, as amended, is patentably distinct and allowance is solicited.

Claims 14-19 are rejected as anticipated by the Lepejian reference. Claims 14-19 remain unamended. Claims 14-19 depend from claim 13, which, as amended, is believed to be patentable. Accordingly, claims 14-19 are believed to be patentable for at least the same reasons claim 13 is believed to be patentable and allowance is solicited.

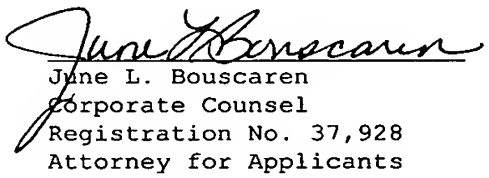
Claim 20 is rejected as anticipated by the Lepejian patent. Claim 20 is amended for clarity, and is otherwise unamended. Claim 20 recites "mapping each generated test code to at least two output lines"...where "only one of said output lines reflects an active value during any one state" and "conjunctively combining respective ones of said output lines with a memory operations signal to generate a memory access enable signal". The Lepejian patent discloses only generation of an address halt signal in response to a memory space exceed condition and does not disclose or suggest the step of mapping test codes to generate "at least two output lines" to provide information as to permissible and impermissible operations. Accordingly, it is believed that claim 20, as amended, is patentably distinct and allowance is solicited.

Claims 21-25 are rejected as anticipated by the Lepejian reference. Claims 21-25 remain unamended. Claims 21-25 depend from claim 20, which, as amended, is believed to be patentable. Accordingly, claims 21-25 are believed to be patentable for at least the same reasons claim 20 is believed to be patentable and allowance is solicited.

If any clarifications can be made by way of telephonic interview, the Examiner is invited to contact the Undersigned.

Respectfully submitted,

Stong et al.
Applicant(s)



June L. Bouscaren
Corporate Counsel
Registration No. 37,928
Attorney for Applicants

Agilent Technologies, Inc.
Legal Dept. DL 432
815 14th St. S.W.
Loveland, CO 80537
Phone: (970) 679-3238
Fax: (970) 679-5772